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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/897,902 | 07/05/2001 | Isamu Hayashi | XA-9512 | 1411 |

181 7590 09/08/2005

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| EXAMINER | |
|---|---|
| LEE, CHRISTOPHER E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2112 | |

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/897,902 | HAYASHI ET AL. | |
| | Examiner | Art Unit | |
| | Christopher E. Lee | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 16th of June 2005. Claims 1, 2, and 7 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Non-Final Office Action was mailed on 16th of February 2005. Currently, claims 1, 2, 6, and 7 are pending in this Application.

### *Claim Rejections - 35 USC § 103*

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakiage [US 5,916,311 A] in view of Yanagiuchi [US 5,684,418 A].

*Referring to claim 1,* Kakiage discloses a microprocessor (i.e., Processor 1 of 1) built on a semiconductor chip (See col. 1, lines 14-35 and col. 3, lines 57-61) comprising:

- a central processing unit (i.e., CPU 2 of Fig. 1) adapted to execute instructions and generate address signals (See col. 10, lines 41-45);
- an external bus interface control circuit (i.e., Bus controller 3 of Fig. 1) coupled to said central processing unit via an internal bus (i.e., CPU 2 is coupled to Bus controller 3 via bus 102-105 in Fig. 1), adapted to control an external bus (i.e., External address bus 123 and External data bus 124 in Fig. 1) based on execution of instructions by said central processing unit (See col. 7, lines 30-35), and being capable of activating one of a plurality of external device select signals (i.e., chip select signals 1201 and 1202 in Fig. 1), which is provided to an outside of said microprocessor (i.e., activated chip select signal is provided to External device 20 or 21 in Fig. 1; See col. 9, lines 12-30) corresponding to said address signals (See col. 7, lines 41-50), wherein

- a first external device (i.e., External device 20 of Fig. 1) which is to be coupled to said microprocessor (i.e., said Processor 1 being coupled said External device 20 when said chip select signal 1201 is activated in Fig. 1),
- a second external device (i.e., External device 21 of Fig. 1) which is to be coupled to said microprocessor (i.e., said Processor 1 being coupled said External device 21 when said chip select signal 1202 is activated in Fig. 1);

- a clock generating circuit (i.e., Frequency synthesizer 4 of Fig. 1), coupled to said central processing unit (i.e., said Frequency synthesizer 4 being coupled to CPU 2 via internal clock signal line 101 in Fig. 1), adapted to generate an internal clock signal (i.e., internal clock signal 101 of Fig. 1); wherein said clock generating circuit (i.e., Frequency synthesizer) provides said internal clock signal (i.e., said internal clock signal) to said central processing unit (i.e., said CPU; See col. 7, lines 35-39).

Kakiage does not teach said clock generating circuit adapted to generate a plurality of clock signals including a first clock signal and a second clock signal; a clock switching control circuit for controlling an operation to switch a synchronous clock signal providing one of said first clock signal and said second clock signal to said external bus interface control circuit in accordance with said external device select signal; a first clock terminal adapted to supply said first clock signal to said first external device; and a second clock terminal adapted to supply said second clock signal to said second external device; wherein said second clock signal has a different frequency from said first clock signal, and wherein said first and second clock signals are output from said microprocessor to said first and second external devices, respectively, in parallel.

Yanagiuchi discloses a clock signal generating system (Fig. 1), wherein

- a clock generating circuit (i.e., clock generator 1 of Fig. 1) adapted to generate a plurality of clock signals (i.e., k number of clock signals in Fig. 1; See col. 1, lines 5-7) including a first clock

signal (e.g., the 1st clock signal of S1, i.e., (S11) in Fig. 11) and a second clock signal (e.g., the ith clock signal of S1, i.e., (S1i) in Fig. 11);

- a clock switching control circuit (i.e., clock selector 2 of Fig. 1) for controlling an operation to switch a synchronous clock signal (i.e., **ck** in Figs. 1 and 11; See col. 9, lines 14-25) providing one of said first clock signal and said second clock signal (i.e., providing said (S11) or (S1i) to functional block in Fig. 11) to an external bus interface control circuit (i.e., latch groups 21 and selectors 22 in Fig. 11) in accordance with an external device select signal (i.e., according to input information of the status signals STS-1 and STS-g in Fig. 11; See col. 9, lines 26-38 and col. 12, lines 40-44);
- a first clock terminal (i.e., a terminal (1) of said clock selector 2 in Fig. 11) adapted to supply said first clock signal to a first external device (e.g., (S11) clock signal to function Block(1) via said terminal(1) in Fig. 11); and
- a second clock terminal (i.e., terminal(g) of said clock selector 2 in Fig. 11) adapted to supply said second clock signal to a second external device (e.g., (S1i) clock signal to function Block(g) via said terminal(g) in Fig. 11), wherein
    - said second clock signal has a different frequency from said first clock signal (i.e., clock signals (S11) and (S1i) having different frequency; See col. 3, line 60 through col. 4, line 8), and said first and second clock signals are output from a microprocessor to said first and second external devices, respectively, in parallel (See Figs. 1 and 11; in fact, said clock signals (S11) and (S1i) are output from hardware in Fig. 1 via clock selectors 22-1 and 22-g as S2-1 and S2-g to said function Block(1) and function Block(g), respectively, in parallel, apparently implies that said first and second clock signals are output from a microprocessor to said first and second external devices, respectively, in parallel).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock generating circuit, as disclosed by Kakiage, for the advantage of providing said clock generating circuit (i.e., clock signal generator) which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

However, the recitation in the preamble, such that "a microprocessor built on a semiconductor chip", has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

*Referring to claim 2,* Kakiage discloses a microprocessor (i.e., Processor 1 of 1) comprising:

- a central processing unit (i.e., CPU 2 of Fig. 1) for executing instructions and generating at least one external access address (See col. 10, lines 41-45);
- an external bus interface control circuit (i.e., Bus controller 3 of Fig. 1) which controls an external bus (i.e., External address bus 123 and External data bus 124 in Fig. 1) based on execution of said instructions by said central processing unit (See col. 7, lines 30-35),
    - wherein said external bus interface control circuit (i.e., said Bus controller) is capable of activating either a first external device select signal (i.e., chip select signal 1201 of Fig. 1) or a second external device select signal (i.e., chip select signal 1202 of Fig. 1) corresponding to said external access address (See col. 7, lines 41-50),

- wherein said microprocessor (i.e., said Processor) includes a clock pulse generator (i.e., Frequency synthesizer 4 of Fig. 1) generating an internal clock signal (i.e., internal clock signal 101 of Fig. 1), and
- wherein said clock pulse generator (i.e., said Frequency synthesizer) provides said internal clock signal (i.e., said internal clock signal) to said central processing unit (i.e., said CPU; See col. 7, lines 35-39).

Kakiage does not teach said microprocessor including a clock switching control circuit, wherein said clock switching control circuit controls an operation to switch a synchronous clock signal of said external bus interface control circuit to one of a first clock signal in accordance with activation of said first external device select signal and a second clock signal in accordance with activation of said second external device select signal, wherein said clock pulse generator generates said first clock signal, said second clock signal, wherein said first clock signal has a predetermined frequency different from that of said second clock signal, and wherein microprocessor includes first and second external clock output terminals outputting said first and second clock signals, respectively, in parallel.

Yanagiuchi discloses a clock signal generating system (Fig. 1), wherein

- a microprocessor (i.e., hardware in Fig. 1) including a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein said clock switching control circuit (i.e., clock selector) controls an operation to switch a synchronous clock signal (i.e., **ck** in Figs. 1 and 11; See col. 9, lines 14-25) of an external bus interface control circuit (i.e., latch groups 21 and selectors 22 in Fig. 11) to one of a first clock signal (e.g., the 1$^{st}$ clock signal of S1, i.e., (S11) in Fig. 11) in accordance with activation of a first external device select signal (e.g., status signal STS-1 for a function Block(1) in Fig. 11) and a second clock signal (e.g., the i$^{th}$ clock signal of S1, i.e., (S1i) in Fig. 11) in accordance with activation of a second external device select signal (e.g., status signal STS-g for a function Block(g) in Fig. 11; in fact, providing said (S11) or (S1i) for functional Block to latch

groups 21 and selectors 22 according to input information of the status signals STS-1 and STS-g in Fig. 11; See col. 9, lines 26-38 and col. 12, lines 40-44),

- wherein a clock pulse generator (i.e., clock generator 1 of Fig. 1) generates said first clock signal and said second clock signal (i.e., the 1st clock signal (S11) and ith clock signal (S1i) in Fig. 11), said first clock signal having a predetermined frequency different from that of said second clock signal (i.e., clock signals (S11) and (S1i) having different frequency; See col. 3, line 60 through col. 4, line 8), and
- wherein said microprocessor includes first and second external clock output terminals (i.e., a terminal (1) and a terminal (g) of said clock selector 2 in Fig. 11) outputting said first and second clock signals, respectively, in parallel (See Figs. 1 and 11; in fact, said clock signals (S11) and (S1i) are output from hardware in Fig. 1 via clock selectors 22-1 and 22-g as S2-1 and S2-g to said function Block(1) and function Block(g), respectively, in parallel, apparently implies outputting said first and second clock signals, respectively, in parallel).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator, as disclosed by Kakiage, for the advantage of providing said clock pulse generator (i.e., clock signal generator) which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

4. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakiage [US 5,916,311 A] in view of Yanagiuchi [US 5,684,418 A] as applied to claims 1 and 2 above, and further in view of Fujita [US 6,529,083 B2].

*Referring to claim 6,* Kakiage, as modified by Yanagiuchi, discloses all the limitations of the claim 6, except that does not teach said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and wherein said clock switching control circuit is further capable of switching said synchronous clock signal, which is provided to said external bus interface control circuit, after an acknowledgment of said request to suspend instruction execution.

Fujita discloses a clock control circuit (See Abstract), wherein

- a clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) requests a central processing unit to suspend execution of instructions in response to activation of a selected external device select signal (i.e., starting the processing for changing the clocks; See col. 8, lines 10-21), and
    - wherein said clock switching control circuit (i.e., clock state control circuit) is further capable of switching a synchronous clock signal (See col. 9, lines 25-32), which is provided to an external bus interface control circuit (i.e., frequency-divided clock control device 10, 11 and 12 in Fig. 1), after an acknowledgment of said request to suspend instruction execution (See col. 9, 17-24; i.e., wherein in fact that the clock state control circuit stops the operation once, and enters the sleeping state implies that said capability of controlling to switch a first clock signal after an acknowledgment of a request for suspending of said instruction execution. In other words, the clock state control circuit is waiting for the CPU acknowledgement of a request for stopping the operation during the sleeping state).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock state control circuit, as disclosed by Fujita, in said clock switching control circuit, as disclosed by Kakiage, as modified by Yanagiuchi, for the advantage of reducing complication in control over operating clock in said clock switching control circuit (i.e., clock control circuit) and realizing more precise and accurate control over an operating speed (See Fujita, col. 10, lines 57-60).

*Referring to claim 7,* Kakiage, as modified by Yanagiuchi and Fujita teaches

- said clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1; Fujita) is capable of switching said internal clock signal (i.e., internal clock signal 101 of Fig. 1; Kakiage) of said central processing unit (i.e., CPU 2 of Fig. 1; Kakiage) in accordance with switching said synchronous clock signal of said external bus interface control circuit (i.e., by way of changing clock source of frequency-divided clock control device; See Fujita, col. 9, lines 33-54).

***Response to Arguments***

5. Applicants' arguments filed on 16th of June 2005 (hereinafter the Response) have been fully considered but they are not persuasive.

*In response to the Applicants' argument with respect to* "... While Kakiage is directed toward a bus controller and information processing device, Kakiage does not teach or suggest the above combination of features found in independent Claims 1 or 2. ... As can be seen from Fig. 1 of Kakiage, the external clock signal 100 is supplied directly to the frequency synthesizer 4, the external device 21 and the access controlling signal generator 8. Not only does Kakiage not generate the first, second and internal clock signals as recited in the independent claims, but Kakiage also does not teach or suggest that the first and second clock signals are output in parallel. Moreover, Kakiage does not disclose that the

second clock signal has a different frequency from said first clock signal as recited in independent Claim 1 nor that the first clock signal has a predetermined frequency different from that of the second clock signal as recited in independent Claim 2. ..." in the Response pages 6-8, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, Kakiage clearly teaches a clock generating circuit (i.e., Frequency synthesizer) providing an internal clock signal to a central processing unit (i.e., CPU; See col. 7, lines 35-39).

Furthermore, the Examiner believes that the Applicants misinterpret the claim rejection. The Applicants essentially argue that Kakiage does not teach said clock generating circuit generates the first and the second clock signals, and the first and second clock signals are output in parallel. However, Yanagiuchi suggests the above argued elements, and the combination of the references Kakiage and Yanagiuchi with rationale suggests all the limitations of the claimed invention (See paragraph 3 of the instant Office Action, claims 1 and 2 rejection under 35 U.S.C. 103(a) as being unpatentable over Kakiage in view of Yanagiuchi).

Thus, the Applicants' argument on this point is not persuasive.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/CEL

TIM VO
PRIMARY EXAMINER